Dr Yashvir Singh

Professor

Department of Electronics & Communication Engineering

Qualifications: *Ph. D, M. Tech, B. Sc Engg.*

Area of Interest: *Solid State Devices*

Contact No.: *9411126345*

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Educational Qualifications:

- Ph.D. in Design, Modeling and Simulation of Semiconductor Devices, Indian Institute of Technology Delhi, New Delhi, India, 2002.
- M.Tech. in Electronics & Communication Engineering, Indian Institute of Technology Roorkee, Roorkee, India, 1991.
- B.Sc. Engg. in Electronics & Communication Engineering, Aligarh Muslim University, Aligarh, India, 1989.
- **Award:** Certificate from IIT Roorkee in 1991 for standing first in M. Tech.

Work Experience:

- Professor, Department of Electronics & Communication Engineering, G.B Pant Institute of Engineering and Technology, Pauri-Garhwal (UK), India from 20th Sep 2005 to present.
- Associate Professor, Department of Electronics & Communication Engineering, G.B Pant Institute of Engineering and Technology, Pauri-Garhwal (UK), India from 20th Sep 1997 to 19th Sep 2005.
- Assistant Professor, Department of Electronics & Communication Engineering, G.B Pant Institute of Engineering and Technology, Pauri-Garhwal (UK), India from 28th Feb 1992 to 19th Sep 1997.

Administrative Experience:

1. Director, G B Pant Institute of Engineering & Technology, Pauri, from Oct 21 to till date.
2. Head, Department of Electronics & Communication Engineering, G B Pant Institute of Engineering & Technology, Pauri, from Sep 16 to Oct 21.
3. Principal, G B Pant Institute of Engineering & Technology, Pauri, from 15 July 2016 to 25 Aug 2016.
4. Principal, G B Pant Institute of Engineering & Technology, Pauri, from 04 Jan 2016 to 16 May 2016.
5. Dean (PG & R), G B Pant Institute of Engineering & Technology, Pauri, from Feb 2014 to Sep 2016.

6. Dean (Academics), G B Pant Institute of Engineering & Technology, Pauri, from May 2009 to Feb 2014.
7. Head, Department of Electronics & Communication Engineering, G B Pant Institute of Engineering & Technology, Pauri, from Mar 2009 to Jan 2016.
8. Principal, G B Pant Institute of Engineering & Technology, Pauri, from Apr 2003 to Oct 2004.
9. Head, Department of Department of Electronics & Communication Engineering, G B Pant Institute of Engineering & Technology, Pauri, from Jul 2003 to Jun 2004.
10. Proctor, G B Pant Institute of Engineering & Technology, Pauri, from Aug 1997 to Jul 1999.
11. Head, Department of Electronics & Communication Engineering, G B Pant Institute of Engineering & Technology, Pauri, from Mar 1992 to Jul 1998.
12. Hostel Warden, G B Pant Institute of Engineering & Technology, from Mar 1992 to Jul 1999.
13. Expert member, Board of Studies, Department of Electronics & Communication Engineering, School of Engineering, HNB Garhwal University, Srinagar, Uttarakhand, India.

Subjects Taught:

1. Basic Electronics Engineering
2. Analog Electronics Circuits
3. IC Technology
4. Analog Integrated Circuits
5. Electronic Devices
6. Analog Circuits

Area of Research:

- Modeling and Simulation of Semiconductor Devices

  Google Scholar Profile: Citations: 447, h index: 13, i17 index: 9 on 8th Jul, 2022.
  (Link: https://scholar.google.com/citations?user=3icDSkUAAAAJ&hl=en)

Research Publications:

International Journals:

1. M S Adhikari, R Patel, Y K Verma and **Y Singh**, " Implementation of Low Voltage MOSFET and Power LDMOS on InGaAs, "Silicon, online, May 2021.
2. Sandeep Kumar, Balraj Singh and **Yashvir Singh** “Analytical Model of Dielectric Modulated Trench Double Gate Junctionless FET for Biosensing Applications," IEEE Sensors Journal, online, Feb 2021.
3. M S Adhikari, Raju Patel, Suman Lata Tripathi and **Yashvir Singh**, “Design of SOI MOSFETs for Analog/RF Circuits,"Indian Journal of Pure & Applied Physics”, Vol. 58, No. 4, pp. 678-685, Sep 2020.

4. Aanchal Garg, Balraj Singh and **Yashvir Singh** "Dual-Gate Junctionless FET on SOI for High Frequency Analog Applications," **Silicon,** online, Aug 2020.
5. Sandeep Kumar, **Yashvir Singh** and Balraj Singh "Extended Source Double-Gate Tunnel FET based Biosensor with Dual Sensing Capabilities", **Silicon,** online, Jun 2020.
6. Sandeep Kumar, **Yashvir Singh** and Balraj Singh and P K Tiwari "Simulation Study of Dielectric Modulated Dual Channel Trench Gate TFET Based Biosensor," **IEEE Sensors Journal,** online, Jun 2020.
7. Aanchal Garg, **Yashvir Singh** and Balraj Singh "Dual-Channel Junctionless FETs for Improved Analog/RF Performance," **Silicon,** online, Jun 2020.
8. Tripuresh Joshi, Balraj Singh and **Y Singh**, "Controlling Ambipolar Current in Ultra-thin SOI TFET using Back-Bias," **Journal of Computational Electronics,** online, Mar 2020.
9. Aanchal Garg, Balraj Singh and **Yashvir Singh** "A New Trench Double Gate Junctionless FET: A Device for Switching and Analog/RF Applications, "**International Journal of Electronics and Communications (AEU),** online, Mar 2020.
10. Tripuresh Joshi, **Y Singh** and Balraj Singh "Extended Source Double-Gate Tunnel FET with Improved DC and Analog /RF Performance," **IEEE Trans. On Electron Devices,** online, Mar 2020.
11. Tripuresh Joshi, **Y Singh** and Balraj Singh "Dual-Channel Trench-Gate (DCTG) Tunnel FET for Improved ON-current and Subthreshold Swing," **Electronics Letters,** online, Aug. 2019.
12. Manoj Singh Adhikari, Raju Patel and **Yashvir Singh**, "High performance dual-gate SiGe MOSFET for radio-frequency applications,"**International Journal of Electronics and Communications (AEU),** Vol. 110, No. 4, pp. 152828, 2019.
13. A. R. Verma and **Y. Singh**, "Adaptive Artifact Cancelation Based on Bacteria Foraging Optimization for ECG Signal,"**Augmented Human Research,** Vol. 4, No. 1, pp. 4, 2019.
14. A. R. Verma and **Yashvir Singh**, "Design of the Multi-Channel Cosine-Modulated Filter Bank Using the Bacterial Foraging Optimization Algorithm," **IETE Journal of Education,** Vol. 59, No. 1, pp. 39-50, 2018.
15. Manoj Singh Adhikari and **Yashvir Singh**, "Implementation of Trench-based Power LDMOS and Low Voltage MOSFET on InGaAs," **IETE Technical Review,** Vol. 36, No. 3, pp. 234-242, 2019.
16. A. R. Verma, **Y. Singh and B. Gupta**, "Adaptive Filtering Method for EMG Signal using Bounded Range Artificial Bee Colony Algorithm," **Biomedical Engineering Letters,** Vol. 8, No. 2, pp. 231-238, 2018.
17. Mohit Payal and **Yashvir Singh**, "A New RF Trench-Gate Multi-Channel Laterally-Diffused MOSFET on InGaAs," **Journal of Semiconductors,** Vol. 92, No. 2, pp. 151-157, 2018.
18. Mohit Payal and **Yashvir Singh**, "RF dual-gate-trench LDMOS on InGaAs with improved performance," **Indian Journal Physics,** Vol. 92, No. 2, pp. 151-157, 2018.

19. Mayank Punetha and **Yashvir Singh**, "SOI Dual-Gate Trench LDMOSFET for RF Integrated Power Amplifiers," **IETE Technical Review,** Vol. 34, No. 4, pp. 431-439, 2017.

20. Mohit Payal and **Yashvir Singh**, "A Multi-Channel Trench-Gate (MCTG) RF LDMOS on SOI," **IETE Technical Review,** Vol. 34, No. 3, pp. 246-253, 2017.

21. A. R. Verma and **Y. Singh**, "Optimization of Two Channel QMF Bank Using Modified Cuckoo Search Technique for Biomedical Image Applications" **International Journal of biomedical Engineering and Technology**, Vol. 24, No. 1, pp. 90-102, 2017.

22. A. R. Verma, **Y. Singh** and Vivek Joshi, "Removing ECG Noise from EMG Signal using Adaptive Artifact Canceller Based on Modify Cuckoo Search Algorithm" **Journal of Basic and Applied Research International**, Vol. 19, No. 2 pp. 91-98, 2016.

23. **Yashvir Singh** and Deepak Dwivedi, "A Power Dual-Gate Laterally-Diffused MOSFET on 4H-SiC," **International Journal of Electronics Letters,** Vol. 5, No. 4, pp. 385-394, 2017.

24. Manoj Singh Adhikari and **Yashvir Singh**, "High performance multi-channel MOSFET on InGaAs for RF amplifiers," **Superlattices and Microstructures,** Vol. 102, pp. 79-87, 2017.

25. Manoj Singh Adhikari and **Yashvir Singh**, "High performance multi-finger MOSFET on SOI for RF amplifiers, "**Indian Journal of Physics,** Vol. 91, No. 10, pp. 1211-1217, 2017.

26. Mohit Payal and **Yashvir Singh**, "A new RF trench-gate multi-channel laterally-diffused MOSFET on InGaAs, "**Journal of Semiconductors,** Vol. 38, No. 9, pp. 94001, 2017.

27. A. R. Verma, **Y. Singh** and Vivek Joshi, "Adaptive Filtering using PSO, MPSO and ABC Algorithms for ECG signal" **International Journal of biomedical Engineering and Technology**, Vol. 4, pp. 379-392, 2016.

28. Vivek Joshi, A. R. Verma, and **Y. Singh**, "De-noising of ECG signal using Adaptive Filter based on MPSO, "**Procedia Computer Science**, Vol. 57, pp. 375-402, 2015.

29. Shivika Goyal, Shefali Goswamy, Akanksha Negi, Aayushi Tomar, A. R. Verma and **Y. Singh**, "Design of ANC Filter Using Modified Cuckoo Search Technique for ECG Signal Enhancement"**, ELSEVIER Journal-Perspectives in Science**, Vol. 8, pp. 43-45, 2016.

30. Mayank Punetha and **Yashvir Singh**, "Dual-channel trench LDMOS on SOI for RF power amplifier Applications," **Journal of Computational Electronics,** Vol. 15, No. 2, pp. 639-645, 2016.

31. Manoj Singh Adhikari and **Yashvir Singh**, "A Nanoscale Dual-Channel Trench (DCT) MOSFET for Analog/RF Applications," **Superlattices and Microstructures,** Vol. 88, pp. 567-573, 2015.

32. Mayank Punetha and **Yashvir Singh**, "A 100-V High-Performance SOI Trench LDMOS with Low Cell Pitch, "**Journal of Electronic Materials,** Vol. 44, No. 10, pp 3388-3394, 2015.

33. Manoj Singh Adhikari and **Yashvir Singh**, "High performance DCTG-LDMOS on InGaAs for RF power amplifier applications," **Material Science in Semiconductor Processing,** Vol. 40, pp 861-866, 2015.

34. Manoj Singh Adhikari and **Yashvir Singh**, “High-performance dual-channel InGaAs MOSFET for small signal RF applications,” **Electronics Letters,** Vol. 51, pp 1203-1205, 2015.

35. **Yashvir Singh** and Mukesh Badiyari, “Performance optimization of InGaAs power LDMOSFET,” **Microelectronics Journal,** Vol. 46, No. 5, pp 404-409 2015.

36. **Yashvir Singh** and Rahul Singh Rawat, “High figure-of-merit SOI power LDMOS for power integrated circuits, ”**Engineering Science and Technology, an International Journal,** Vol. 18, No. 2, pp. 141-149 2015.

37. **Yashvir Singh** and Prashant Naithani, “Lateral trench oxide Schottky rectifier on SOI for power integrated circuits,**” Journal of Computational Electronics,** Vol. 13, No.4, pp.965-970, 2014.

38. **Yashvir Singh** and Mayank Joshi, "Simulation Study of Lateral Trench Gate Power MOSFET on 4H-SiC, "**International Journal of Electrical, Computer, Energetic, Electronics & Communication Engineering,** Vol.8, No.2, pp. 369-372, 2014.

39. **Yashvir Singh** and Swati Chamoli, "Effect of Field Dielectric Material on Performance of InGaAs Power LDMOSFET, "**International Journal of Electrical, Computer, Energetic, Electronics & Communication Engineering,** Vol.7 No.8, pp.1087-1090, Aug 2013.

40. **Yashvir Singh** and Manoj Singh Adhikari, "Performance evaluation of a lateral trench-gate power MOSFET on InGaAs,” **Journal of Computational Electronics,** Vol. 13, No.1, pp.155-160, 2014.

41. **Yashvir Singh** and Mayank Punetha, "A Lateral Trench Dual Gate Power MOSFET on Thin SOI for Improved Performance, **“Journal of Solid State Science and Technology,** Vol. 2, No. 7, pp.Q113-Q117, May 2013.

42. Meena Mishra, M. Jagadesh Kumar, **Yashvir Singh**, S.R Shukla, H.P. Vyas, D.S. Rawal, A. Naik, H.S. Sharma, B.K. Sehgal and R. Gulati, "Inverse Modeling of Delta Doped PHEMTs," **Journal of Vacuum Science & Technology A**, Vol.22, No. 3, pp.1036-1039, Jun 2004.

43. M. Jagadesh Kumar and **Yashvir Singh**, "Lateral Schottky Rectifiers for Power Integrated Circuits," **SPIE proceedings series**, Vol.1, pp.414-421, 2002.

44. M. Jagadesh Kumar and **Yashvir Singh**, "A New Lateral Trench Sidewall Schottky (LTSS) Rectifier on SOI with High and Sharp Breakdown Voltage," **IEEE Trans. On Electron Devices,** Vol.49, pp.1316-1319, 2002.

45. **Yashvir Singh** and M. Jagadesh Kumar, "Lateral Thin Film Schottky (LTFS) Rectifier on SOI: A Device with Higher than Plane Parallel Breakdown Voltage," **IEEE Trans. On Electron Devices**, Vol.49, pp.181-184, 2002.

46. **Yashvir Singh** and M. Jagadesh Kumar, "A New 4H-SiC Lateral Merged Double Schottky (LMDS) Rectifier with Excellent Forward and Reverse Characteristics,” **IEEE Trans. On Electron Devices**, Vol.48, pp.2695-2700, Dec 2001.

47. **Yashvir Singh** and M. Jagadesh Kumar, "Novel Lateral Merged Double Schottky (LMDS) Rectifier: Proposal and Design," **IEE Proceedings - Circuits, Devices and Systems**, Vol.148, No.3, pp.165-170, June 2001.

International Conferences:

1. Aanchal Garg, Yashvir Singh, Balraj Singh "Performance Optimization of Vertical Gaussian Doped SOI Junctionless FET with Substrate Bias Effects", **IEEE International Conference on Electrical and Computer Engineering (WITCON ECE),** pp. 223-226, WIT, Dehradun, India, Nov 2019.
2. Aanchal Garg and Y. Singh "Nanoscale SiGe Double Gate MOSFET (DG-MOSFET) for Analog/RF Circuits", **IEEE International Conference on Electrical, Electronics and Computer Engineering,** pp. 1-3, AMU, Aligarh, India, 7-9 Nov 2019.
3. S. Kumar, R. Sharma, M. A. Rahman, R. K Jha, Neha, Shreya, A. R. Verma and Y. Singh "Robust Secret Sharing for Image Encryption in Fractional Fourier Transform Domain", **IEEE International Conference on Computing, Power and Communication Technologies**, pp. 497-502, NCR, New Delhi, India, 27-28 Sep 2019.
4. Sumit Kumar, R K Jha, R Sharma, A. R. Verma and Y. Singh "A Robust Sharing Based Encryption Method in Singular Value Decomposition Domain using Fractional Fourier Transform", **IEEE 8th International Symposium on Embedded Computing & System Design,** pp. 135-140, Kochi, India, 13-15 Dec 2018.
5. Manoj Singh Adhikari and **Yashvir Singh**, "80V InGaAs Lateral Trench Power MOSFET", **IEEE International Conference on Computational Techniques in Information and Communication Technologies,** New Delhi, India, 11-13 Mar 2016.
6. A. R. Verma and Y. Singh "Design of Two-channel QMF bank based on Cuckoo Search Algorithm", **IEEE 3rd International Conference on Signal Processing & Integrated Networks,** Noida, India, Mar 2016.
7. Manoj Singh Adhikari and **Yashvir Singh**, "Simulation of Trench-based InGaAs LDMOSFET with Improved Performance", **IEEE International Conference on Electrical, Computer and Electronics (UPCON 2015),** Allahabad, India, 1-2 Apr 2015.
8. Mayank Punetha, **Yashvir Singh**, and Shardul Thapliyal "A Vertical Super-Junction Strained-Silicon Channel Power MOSFET," **IEEE International Conference (TENCON 2015)**, Macau, China, 1-4 Nov 2015.
9. Mayank Punetha and **Yashvir Singh**, "An Integrable Trench LDMOS Transistor on SOI for RF Power Amplifiers in PICs," **19th International Symposium on VLSI Design and Test (VDAT-2015)**, Ahmedabad, India, 26-29 June 2015.
10. **Yashvir Singh**, Shardul Thapliyal "Implementation of Trench Schottky Barrier diodes on InGaAs for Power Integrated Circuits," **2nd IEEE International Conference on Advances in Computing & Communication Engineering,** Dehradun, India, pp. 183-186, 1-2 May 2015.

11. **Yashvir Singh**, Deepak Dwivedi “Simulation Study of Dual-Gate Trench LDMOSFET on 4H-SiC," **2nd IEEE International Conference on Advances in Computing & Communication Engineering,** Dehradun, India, pp. 174-177, 1-2 May 2015.
12. Manoj Singh Adhikari, **Yashvir Singh**, “Performance Enhancement of InGaAs MOSFET using Trench Technology," **International Conference on Signal Processing and Communication,** Noida, India, pp. 309-311, 16-18 Mar 2015.
13. Vivek Joshi, A. R. Verma, **Y. Singh**, “De-noising of ECG Signal using Adaptive Filter based on MPSO," **Third International Conference on Recent Trends in Computing,** Delhi, India, 12-13 Mar 2015, **Elsevier** 7 (2015) *395-402,* **ISSN: 1877-0509.**
14. A. R. Verma, **Y. Singh**, “Adaptive Tunable Notch Filter for ECG Signal Enhancement," **Third International Conference on Recent Trends in Computing,** Delhi, India, 12-13 Mar 2015, **Elsevier** 7 (2015) 332 – 337, **ISSN: 1877-0509**
15. A. R. Verma, B. S. Ghugtyal, **Y. Singh** and V. Joshi, “An Optimization Technique for QMF Based on Modified Particle Swarm," **2nd International Conference on Signal Processing & Integrated Networks,** Noida, India, 19-20 Feb 2015, pp: 666 – 669, **IEEE**. **ISBN:** 978-1-4799-5990-7.
16. Mohit Payal and **Yashvir Singh**, “A New Lateral Dual Gate Power MOSFET on InGaAs with Improved Performance," **1st International Conference on Microelectronics, Circuit and Systems,** Kolkata, India, 11-13 July 2014.
17. **Yashvir Singh** and Mukesh Badiyari, "74V High-Figure-of-Merit Lateral Trench Gate Power MOSFET on InGaAs**, "International Conference on Advances in Engineering & Technology,** Roorkee, India, 24-25 May 2014.
18. Mayank Punetha and **Yashvir Singh**, "Performance Enhancement of SOI power LDMOSFET using Trench Gate Technology," **IEEE International Conference on Recent Advances & Innovations in Engineering,** Jaipur, India, 9-11 May 2014.
19. Mayank Punetha and **Yashvir Singh**, "A 90 V Integrable Lateral Trench Power MOSFET on SOI**, "IEEE International Conference on Advances in Engineering and Technology,** Nagapattinam, India, 2-3 May 2014.
20. **Yashvir Singh** and Prashant Naithani, "Simulation of Lateral Trench Oxide Schottky Rectifier on SOI for Power Integrated Circuits," **International Conference on Innovative Advancements in Engineering and Technology,** JNU, Jaipur, India, 7-8 Mar 2014.
21. Mohit Payal and **Yashvir Singh**, "Simulation of a Lateral Trench Power MOSFET on InGaAs for Improved Performance," **International Conference on Recent Advances in Engineering and Computational Science,** Chandigarh, India, 6-8 Mar 2014.
22. A. R. Verma, **Y. Singh** and A. K. Gautam, "A comparative study of Different Transforms and ANFIS for speech Enhancement based on Hybrid Learning Algorithm," **International Conference on Advances in Computing & Communication Engineering,** Almora, India, 22-23 Feb 2014.

23. **Yashvir Singh** and Rahul Singh Rawat, "Simulation of Lateral Trench Gate MOSFET on SOI for Power Integrated Circuits," **International Conference on Advances in Computing & Communication Engineering,** Almora, India, 22-23 Feb 2014.
24. **Yashvir Singh** and Manoj Singh Adhikari, "Lateral Trench Gate InGaAs Power MOSFET," **International Conference on Communication Systems,** Pilani, India, 18-20 Oct 2013.
25. **Yashvir Singh** and Mayank Joshi, "High Performance 4H-SiC Power MOSFET," **International Conference on Communication Systems,** Pilani, India, 18-20 Oct 2013.
26. **Yashvir Singh** and Mohit Payal, “Simulation of Recessed-Gate AlGaN-GaN DH-HEMT for Power Electronics Applications”, **World Conference on Advances in Communications and Control Systems,** Dehradun, India, 6-8 Apr 2013.
27. **Yashvir Singh** and Mayank Punetha, "High Performance SOI Lateral Trench Dual Gate Power MOSFET," **International Conference on Communications, Devices and Intelligent Systems,** Kolkata, India, pp. 137-140, 28-29 Dec 2012.
28. M. Mishra, **Y. Singh**, S.S. Islam, S.R Shukla, M. Jagadesh Kumar, A. Naik, B.K. Sehgal and R. Gulati, H.P. Vyas, "Inverse Modeling of Delta-doped PHEMTs, "**Eleventh Canadian Semiconductor Technology Conference,** Ottawa, Canada, 18-22 Aug 2003.
29. **Y. Singh** and M. Jagadesh Kumar, "A New Lateral Trench Sidewall Schottky Rectifier on SOI, "**Technical Proceedings of the Nanotech 2002, International Conference on Modeling and Simulation of Microsystems**, Vol.1, pp.592-595, San Juan, Puerto Rico, U.S.A., Apr 2002.
30. **Y. Singh**, M. Jagadesh Kumar, S.R.Shukla, Meena Mishra, and H.P. Vyas, "Study of Pseudomorphic HEMTs using 2D Numerical Simulation Supported by Experimental Data," **11th International Workshop on the Physics of Semiconductor Devices**, Vol.2, pp.1368-1371, Dec 2001.
31. **Y. Singh** and M. Jagadesh Kumar, "Low-loss High-performance Lateral Schottky Rectifiers on SOI," **11th International Workshop on the Physics of Semiconductor Devices**, Vol.2, pp.1382-1385, Dec 2001.
32. M. Jagadesh Kumar and **Y. Singh** (Invited Talk), "Lateral Schottky Rectifiers for Power Integrated Circuits," **11th International Workshop on the Physics of Semiconductor Devices**, Vol.1, pp.414-421, Dec 2001.

Ph. D. Thesis Supervision:

Completed:

1. Mohit Payal, Design and Simulation of RF Power LDMOS on SOI and InGaAs, Nov 2021
2. Tripuresh Joshi, Performance Improvement of TFETs for Switching and Analog/RF Applications, Oct 2021 (with Dr Balraj Singh).
3. Pushpraj Singh Chauhan, Fading Analysis in Wireless Communication Systems with

Diversity Reception, Jul 2021 (with Dr S K Soni).

4. Mayank Punetha, Design and Simulation of Lateral Trench Power MOSFETs on SOI, Jun 2020
5. Manisha Bhatt, Performance Analysis of Wireless Communication Systems over Composite Fading Channel, Feb 2020 (with Dr S K Soni).
6. Manoj Singh Adhikari, Design and Simulation of Small Signal and Power MOSFETs, Jan 2019.
7. Agya Ram Verma, Filter Design Using Evolutionary Optimization Techniques For Biomedical Applications, Jan 2019

In Progress:

1. Sandeep Kumar, Modeling and Simulation of Dielectrically-Modulated TEFT and JFET Based Biosensors (with Dr Balraj Singh).
2. Aanchal Garg, Performance Evaluation of Junctionless FETs for Switching and Analog/RF Applications (with Dr Balraj Singh).

M. Tech. Thesis Supervision:

Completed (2012 onwards)**:**

1. Aanchal Garg, Dual-Gate SiGe MOSFET for Small Signal Analog/RF Applications, 2016.
2. Vatsala Juyal, Lateral Triple Trench Oxide Schottky (LTTOS) Barrier Diode, 2016.
3. Deepak Dwivedi, Simulation of a Dual-Gate Trench LDMOSFET on 4H-SiC, 2015
4. Shardul Thapliyal, Improving Performance of InGaAs Schottky Diode using Trench Technology, 2015.
5. Mukesh Badiyari, High Performance InGaAs MOSFET, 2014
6. Rahul Singh Rawat, High Figure of Merit SOI Power MOSFET, 2014.
7. Prashant Naithani, Lateral Trench Oxide Schottky Rectifier on SOI, 2014
8. Mayank Joshi, A Lateral Trench Gate Power MOSFET on 4H-SiC, 2013.
9. Swati Chamoli, Effect of Dielectric Material on Performance of InGaAs Power MOSFET, 2013
10. Manoj Singh Adhikari, A Lateral Trench Gate InGaAs Power MOSFET, 2013
11. Mayank Punetha, A Novel SOI Lateral Trench Dual Gate Power MOSFET, 2012.
12. Mohit Payal, Simulation of AlGaN/GaN/AlGaN DH-HEMT, 2012
13. Kirti Chaukiyal, Simulation of a Trench Dual Gate MESFET on SOI, 2012

Professional Activities:

Professional Affiliation:

1. Member, the Institute of Electrical and Electronic Engineers (IEEE).

Reviewer in International Journals:

1. IEEE Transactions on Electron Devices
2. International Journal of Electronics and Communications (AEU)
3. IET Electronics Letters
4. Journal of Computational Electronics
5. Superlattices and Microstructures
6. Material Science in Semiconductor Processing
7. Microelectronics Journal
8. International Journal of Electronics
9. Journal of Semiconductors

Short-Term Courses/Faculty Development Programmes/Conferences Organized:

1. **FDP** on “Artificial Intelligence and Machine Learning using Python” Aug 31, - Sep 4, 2020, Department of Electronics and Communication Engineering, GBPIET, Pauri.
2. **FDP** on “ICT Tools for Teaching" Dec 14-18, 2020, Department of Electronics and Communication Engineering, GBPIET, Pauri.
3. **FDP:** on “Recent Research Trends in Electronics and Communication Engineering" Aug 18-28, 2020, Department of Electronics and Communication Engineering, GBPIET, Pauri.
4. **Industrial Training for Students:** on “Current Industry Scenario" Jul 29, Aug 9, 2020, Department of Electronics and Communication Engineering, GBPIET, Pauri.
5. **International Conference:** Smart Machine Intelligence and Real-time Computing, Jun 26-27, 2020, Department of Electronics and Communication Engineering, GBPIET, Pauri.
6. **Workshop:** One-week workshop on "Antenna Design, Fabrication and Measurement Technologies" Nov 25-29, 2019, Department of Electronics and Communication Engineering, GBPIET, Pauri.
7. **Short-Term Course:** One-week short-term course on "FPGA and Mentor Graphics Tool" Oct 10-14, 2019, Department of Electronics and Communication Engineering, GBPIET, Pauri.
8. **Short-Term Course:** One-week short-term course on “Modeling and Simulation of Advanced Semiconductor Devices & VLSI circuits” from 25-29 June 2018 at Department of Electronics and Communication Engineering, GBPIET, Pauri.
9. **Seminar:** Two days seminar on “Recent Trends in Electronic Devices and Signal

Processing” from Oct 10-11, 2017at GBPIET, Pauri Garhwal

Short-Term Courses/Faculty Development Programmes Participated:

1. **STC:** Design of CMOS Operational Amplifier ICs- A unique pedagogical approach, Mar 5-11, 2021, IIT, Gandhinagar.
2. **FDP:** Professional Development Training, Feb 24-26, 2021, IIM, Raipur.
3. **FDP:** VLSI and Nanotechnology in Energy, Environment, and Neuromorphic Computation, Dec 21-23, 2020, IIT, Indore.
4. **Short Term Training Programme:** Expert talk in Advanced VLSI Design and Applications with Hands-on CADENCE Tools, Oct 19-24, 2020, ABES Engineering College, Ghaziabad (UP).
5. **FDP:** Expert talk in “Recent Research Trends in Electronics and Communication Engineering" Aug 18-28, 2020, Department of Electronics and Communication Engineering, GBPIET, Pauri.