Resume

Title	**Dr.**	First Name	**BALRAJ**	Last Name	**SINGH**	
Designation		Associate Professor				
Dept. Name		Electronics and Communication Engineering				
Address:		Type-IV Qtr, Block-F-2,G.B.Pant institute of Engineering and Technology,Pauri Garhwal,Uttarakhand-246194				
Phone No.		7302536620/9457166920				
Email		1. bls10fece@gbpec.ac.in		2. balraj.bits@gmail.com		
Web Page (if any)						
Subjects Taught		Analog Electronics, Microelectronics, Basic Electronics, VLSI Design, Semiconductor Device Modeling, Network Analysis and Synthesis				
Areas of Interest/Specialization		Semiconductor Device Modeling, Nanoscale FETs for CMOS applications				
Experience (in years)		Total	13 Years 8 Months			
		Industry				
		Teaching	13 Years 8 Months			
		Research	10 Years			
Educational Qualifications		UG	B.Tech. in Electronics & Communication Engineering, I.E.T., M.J.P.Rohlkhand University, Bareilly (U.P.), India, 2005.			
		PG	M.E. in Embedded System, Birla Institute of Technology and Science, Pilani, Rajasthan India, 2008.			
		Doctorate	Ph.D. in Electronics Engineering, Indian Institute Technology (Banaras Hindu University) Varanasi (UP)-221005, India, 2017			
		Any other				
Research Publications in Journals		**1.** Gola, D., Duksh, Y.S., **Balraj Singh**. et al. Self-heating and Negative Differential Conductance Improvement by Substrate Bias Voltage in Tri-gate Junctionless Transistor. Silicon 14, 2219–2224 (2022). https://doi.org/10.1007/s12633-021-01019-1. **2.** Aanchal Garg., **Balraj Singh**& Yashvir Singh, Dual-Gate Junctionless FET on SOI for High Frequency Analog Applications. *Silicon* **13,** 2835–2843				

(2021). https://doi.org/10.1007/s12633-020-00609-9. **(Impact Factor: 2.67).**

3. Sandeep Kumar, **Balraj Singh** and Yashvir Singh, "Analytical Model of Dielectric Modulated Trench Double Gate Junctionless FET for Biosensing Applications," in ***IEEE Sensors Journal***, vol. 21, no. 7, pp. 8896-8902, 1 April1, 2021, doi: 10.1109/JSEN.2021.3056385. **(Impact Factor: 3.301).**
4. Sandeep Kumar, Yashvir Singh , **Balraj Singh** , Pramod Kumar Tiwari, "Simulation Study of Dielectric Modulated Dual Channel Trench Gate TFET-Based Biosensor," in ***IEEE Sensors Journal***, vol. 20, no. 21, pp. 12565-12573, 1 Nov.1, 2020, doi: 10.1109/JSEN.2020.3001300. **(Impact Factor: 3.301).**
5. Sandeep Kumar, Yashvir Singh**, Balraj Singh ,** Extended Source Double-Gate Tunnel FET Based Biosensor with Dual Sensing Capabilities. ***Silicon* 13,** 1805–1812 (2021). https://doi.org/10.1007/s12633-020-00565-4 **.(Impact Factor: 2.67).**
6. Aanchal Garg., Yashvir Singh & **Balraj Singh**.Dual-Channel Junctionless FETs for Improved Analog/RF Performance. ***Silicon* 13,** 1499–1507 (2021). https://doi.org/10.1007/s12633-020-00545-8. **(Impact Factor: 2.67).**
7. Yograj Singh Duksh1, **Balraj Singh,** Deepti Gola, Pramod Kumar Tiwari, Satyabrata Jit, Subthreshold Modeling of Graded Channel Double Gate Junctionless FETs. ***Silicon* 13,** 1231–1238 (2021). https://doi.org/10.1007/s12633-020-00514-1. **(Impact Factor: 2.67).**
8. Tripuresh Joshi**, Balraj Singh** and Yashvir Singh. Controlling the ambipolar current in ultrathin SOI tunnel FETs using the back-bias effect. **J Comput Electron** 19, 658–667 (2020). https://doi.org/10.1007/s10825-020-01484-8. **(Impact Factor: 1.807)**
9. Aanchal Garg, **Balraj Sin**gh, Yashvir Singh, A new trench double gate junctionless FET: A device for switching and analog/RF applications, **AEU - International Journal of Electronics and Communications**,Volume 118,2020,153140,ISSN 1434-8411, https://doi.org/10.1016/j.aeue.2020.153140. **(Impact Factor: 3.183)**
10. Tripuresh Joshi, Yashvir Singh and **Balraj Singh**, "Extended-Source Double-Gate Tunnel FET With Improved DC and Analog/RF Performance," in **IEEE Transactions on Electron Devices**, vol. 67, no. 4, pp. 1873-1879, April 2020, doi: 10.1109/TED.2020.2973353. **(Impact**

Factor: 2.917)

11. Tripuresh Joshi, Yashvir Singh and **Balraj Singh,** "Dual-channel trench-gate tunnel FET for improved ON-current and subthreshold swing," in **Electronics Letters**, vol. 55, no. 21, pp. 1152-1155, 17 10 2019, doi: 10.1049/el.2019.2219**. (Impact Factor: 1.59)**
12. Deepti Gola, **Balraj Singh**,Jawar Singh, Satyabrata Jit and Pramod Kumar Tiwari," Static and Quasi-Static Drain Current Modeling of Tri-Gate Junctionless Transistor with Substrate Bias Induced Effects" IEEE Trans. Electron Devices, vol. 66, no. 7, pp. 2876-2883, July 2019, doi: 10.1109/TED.2019.2915294. **(Impact Factor: 2.94).**
13. Deepti Gola, **Balraj Singh**, and Pramod Kumar Tiwari, "Subthreshold Characteristic Analysis and Model for Tri-Gate SOI MOSFETs using Substrate Bias Induced Effects." in **IEEE Transactions on Nanotechnology**, vol. 18, pp.329 -335, 2019. **DOI:** 10.1109/TNANO.2019.2906567. (**Impact Factor: 2.196**).
14. **Balraj Singh**, Trailokya Nath Rai, et all, "Ferro-electric stacked gate oxide heterojunction electro-statically doped source/drain double-gate tunnel field effect transistors: A superior structure," ***Mater. Sci. Semicond. Process.***, vol. 71, pp. 161–165, 2017. doi.org/10.1016/j.mssp.2017.07.014 (**Impact Factor: 3.085**).
15. **Balraj Singh,**, Deepti Gola, Kunal Singh, Ekta Goel, Sanjay Kumar, and Satyabrata Jit "Analytical modeling of subthreshold characteristics of ion-implanted symmetric double gate junctionless field effect transistors," ***Mater. Sci. Semicond. Process***., vol. 58, pp. 82–88, 2017. doi.org/10.1016/j.mssp.2016.10.051 (**Impact Factor: 3.085**).
16. **Balraj Singh,** Deepti Gola , Kunal Singh, Ekta Goel, Sanjay Kumar and Satyabrata Jit "2-D Analytical Threshold Voltage Model for Dielectric Pocket Double-Gate Junctionless FETs by Considering Source/Drain Depletion Effects ," ***IEEE Trans. Electron Devices,*** vol. 64, no. 3, pp. 901–908, 2017. DOI: 10.1109/TED.2016.2646460 (**Impact Factor: 2.94**).
17. **Balraj Singh,** Deepti Gola, Kunal Singh, Ekta Goel, Sanjay. Kumar, and Satyabrata Jit, "Analytical Modeling of Channel Potential and Threshold Voltage of Double-Gate Junctionless FETs With a Vertical Gaussian-Like Doping Profile," ***IEEE Trans. Electron Devices,*** vol. 63, no. 6, pp. 2299–2305, 2016. (**Impact Factor: 2.94**) DOI: 10.1109/TED.2016.2556227.

18. **Balraj Singh,** Deepti Gola, Ekta Goel, Sanjay Kumar, Kunal Singh, and Satyabrata Jit, "Dielectric pocket double gate junctionless FET: a new MOS structure with improved subthreshold characteristics for low power VLSI applications," ***J. Comput. Electron.***, vol. 15, no. 2, pp. 502–507, 2016. (**Impact Factor: 1.526**) DOI: 10.1007/s10825-016-0808-3**.**
19. Deepti Gola, **Balraj Singh,** and P. K. Tiwari," Subthreshold Modeling of Tri-Gate Junctionless Transistors with Variable Channel Edges and Substrate Bias Effects" ***IEEE Trans. Electron Devices*** Volume: 65 , Issue: 5 , May 2018 DOI: 10.1109/TED.2018.2809865 (**Impact Factor: 2.94**).
20. Deepti Gola, **Balraj Singh,** and P. K. Tiwari, "A Threshold Voltage Model of Tri-Gate Junctionless Field-Effect Transistors Including Substrate Bias Effects," ***IEEE Trans. Electron Devices,*** vol. 64, no. 9, pp. 3534–3540, 2017. **DOI: 10.1109/TED.2017.2722044 (Impact Factor: 2.94**).
21. Sanjay Kumar, Kunal Singh, Sweta Chander, Ekta Goel, Prince Kumar Singh, Kamlaksha Baral, **Balraj Singh** and Satyabrata Jit, "2-D Analytical Drain Current Model of Double- Gate Heterojunction TFETs With a SiO2/HfO2 Stacked Gate-Oxide Structure" ***IEEE Trans. Electron Devices*** Volume: 65, Issue: 1, Jan. 2018 . **DOI: 10.1109/TED.2017.2773560** (**Impact Factor: 2.94**).
22. Kunal Singh, Sanjay Kumar, Ekta Goel, **Balraj Singh**, and Satyabrata Jit, "Effects of source/drain elevation and side spacer dielectric on drivability performance of non-abrupt ultra shallow junction gate underlap GAA MOSFETs," ***Indian J. Phys. February 2018, Volume 92, Issue 2, pp 171–176***. doi.org/10.1007/s12648-017-1091-2 (Impact **Factor 0.988**).
23. Ekta Goel, Sanjay Kumar, **Balraj Singh**, Kunal. Singh, and Satyabrata Jit, "Two-dimensional model for subthreshold current and subthreshold swing of graded-channel dual-material double-gate (GCDMDG) MOSFETs," ***Superlattices Microstruct.***, vol. 106, no. April, pp. 147–155, 2017. doi.org/10.1016/j.spmi.2017.03.047 (**Impact Factor: 2.123**)
24. Sanjay Kumar, Ekta Goel, Kunal Singh, **Balraj Singh,** and Prince Kumar Singh and Satyabrata Jit "2-D Analytical Modeling of the Electrical Characteristics of Dual-Material Double- Gate TFETs With a SiO 2 / HfO 2 Stacked Gate-Oxide Structure," ***IEEE Trans. Electron Devices***, vol. 64, no. 3, pp. 960–968, 2017. DOI: 10.1109/TED.2017.2773560 (**Impact Factor: 2.94**)

25. Ekta Goel, Kunal Singh, **Balraj Singh,** Sanjay. Kumar, and Satyabrata Jit, "2-D analytical modeling of subthreshold current and subthreshold swing for ion-implanted strained-Si double-material double-gate (DMDG) MOSFETs," ***Indian J. Phys.***, vol. 91, no. 9, pp. 1069–1076, 2017. DOI: 10.1007/s12648-017-1019-x (**Impact Factor 0.988**)

26. Kunal Singh, Sanjay Kumar, Ekta Goel, **Balraj Singh,** Sarvesh Dubey and Satyabrata Jit, "Effects of Elevated Source/Drain and Side Spacer Dielectric on the Drivability Optimization of Non-abrupt Ultra Shallow Junction Gate Underlap DG MOSFETs," ***J. Electron. Mater.***, vol. 46, no. 1, pp. 520–526, 2017. DOI: 10.1007/s11664-016-4912-8 (**Impact Factor: 1.579**)

27. Ekta Goel, **Balraj Singh,** Sanjay Kumar, Kunal Singh, and Satyabrata Jit "Analytical threshold voltage modeling of ion-implanted strained-Si double-material double-gate (DMDG) MOSFETs," ***Indian J. Phys.***, vol. 91, no. 4, pp. 383–390, 2016. DOI: 10.1007/s12648-016-0918-6 (**Impact Factor 0.988**)

28. Kunal Singh, Sanjay Kumar, Ekta Goel, **Balraj Singh,** Mrigendra Kumar, Sarvesh Dubey and Satyabrata Jit, "Subthreshold Current and Swing Modeling of Gate Underlap DG MOSFETs with a Source/Drain Lateral Gaussian Doping Profile," ***J. Electron. Mater.,*** vol. 46, no. 1, pp. 579–584, 2017. DOI: 10.1007/s11664-016-4914-6 (**Impact Factor: 1.579**)

29. Sanjay Kumar, Ekta Goel, Kunal Singh, **Balraj Singh,** Mrigendra Kumar, and Satyabrata Jit, "A Compact 2-D Analytical Model for Electrical Characteristics of Double-Gate Tunnel Field-Effect Transistors With a SiO 2 / High- k Stacked Gate-Oxide Structure," ***IEEE Trans. Electron Devices***, vol. 63, no. 8, pp. 3291–3299, 2016(**Impact Factor: 2.94**). DOI: 10.1109/TED.2016.2572610

30. Ekta Goel, Sanjay Kumar, Kunal Singh, **Balraj Singh**, Mrigendra Kumar, and Satyabrata Jit,, "2-D Analytical Modeling of Threshold Voltage for Graded-Channel Dual-Material Double-Gate MOSFETs," ***IEEE Trans. Electron Devices,*** vol. 63, no. 3, pp. 966–973, 2016. (**Impact Factor: 2.94**). DOI: 10.1109/TED.2016.2520096

31. Mrigendra Kumar, Sanjay Kumar, Ekta. Goel, Kunal Singh, Balraj Singh, and Satyabrata Jit "Strain-Induced Plasma Radiation in Terahertz Domain in Strained-Si-on-Insulator MOSFETs," ***IEEE Trans. Plasma Sci.***, Volume: 44 , Issue: 3 , March 2016 pp. 245–249, 2016. (**Impact Factor: 1.252**).

	DOI: 10.1109/TPS.2016.2516588 **32.** Kunal Singh, Sanjay Kumar, Ekta Goel, Balraj Singh, Mrigendra Kumar, S. Dubey, and S. Jit, "Analytical Modeling of Potential Distribution and Threshold Voltage of Gate Underlap DG MOSFETs with a Source/Drain Lateral Gaussian Doping Profile," ***J. Electron. Mater.***, vol. 45, no. 4, pp. 2184–2192, 2016. (**Impact Factor: 1.579**) DOI: 10.1007/s11664-015-4254-y **33.** Brajesh Kumar Kaushik, S.K.Verma, and **Balraj Singh**, "Encoding in VLSI Interconnects," in ***Communications in Computer and Information Science***, vol. 154, no. January, 2011, pp. 260–269. DOI: 10.1007/978-3-642-21153-9_24
Papers Published in Conference Proceedings	**1.** Tripuresh Joshi Yashvir Singh and **Balraj Singh** "A simulation Study of Double Channel Trench gate Tunnel FET for Analog Applications" IEEE International conference on Advances in Computing, Communication & Materials (ICACCM-2020) at Tula's Institute Dehradun, India, August 21-22, 2020. **2.** A. Garg, Y. Singh and **Balraj Singh**, "Performance Optimization of Vertical Gaussian Doped SOI Junctionless FET with Substrate Bias Effects," IEEE, 2019 Women Institute of Technology Conference on Electrical and Computer Engineering (WITCON ECE), Dehradun Uttarakhand, India, 2019, pp. 223-226, doi: 10.1109/WITCONECE48374.2019.9092931. **3.** D. Gola, **Balraj Singh**, and P. K. Tiwari, "Analytical Modeling of Analog/RF Parameters for Trigate Junctionless Field Effect Transistor Incorporating Substrate Biasing Effects," TENCON 2019 - 2019 IEEE Region 10 Conference (TENCON), Kochi, India, 2019, pp. 1838-1841, doi: 10.1109/TENCON.2019.8929248. **4.** **Balraj Singh**, D. Gola and S. Jit, "Subthreshold Performance Analysis of Double-Fin Multi-channel Junctionless Transistor with Substrate Bias Effects," TENCON 2019 - 2019 IEEE Region 10 Conference (TENCON), Kochi, India, 2019, pp. 1834-1837, doi: 10.1109/TENCON.2019.8929269. **5.** **Balraj Singh** and Satyabrata Jit,"Performance Investigation of Cylindrical

Double Gate Junctionless FET" 2018 5th IEEE Uttar Pradesh Section International Conference on Electrical, Electronics and Computer Engineering (UPCON), Date of Conference: 2-4 Nov. 2018, DOI: 10.1109/UPCON.2018.8596924.

6. Sanjay Kumar, Kamalaksha Baral, Sweta Chander, Prince Kumar Singh, **Balraj Singh,** and Satyabrata Jit, " Performance Evaluation of Double Gate III-V Heterojunction Tunnel FETs with SiO2/HfO2 Gate Oxide Structure " in the proceedings of 2018, IEEE International Symposium on Devices, Circuits and Systems, **ISDCS** 2018 DOI: 10.1109/ISDCS.2018.8379681.

7. **Balraj Singh,** Deepti Gola, Kunal Singh, Ekta Goel, Sanjay Kumar, and Satyabrata Jit, "Temperature Sensitivity Analysis of Double Gate Junctionless Field Effect Transistor with Vertical Gaussian Doping Profile," in the proceedings of 2016 **IEEE** *International Conference on Micro-Electronics and Telecommunication Engineering (ICMETE)*, 2016, pp. 675–679. DOI: 10.1109/ICMETE.2016.127.

8. **Balraj Singh**, Deepti Gola, Kunal Singh, Ekta Goel, Sanjay Kumar, and Satyabrata Jit, "Performance Evaluation of Double Gate Junctionless Field Effect Transistor with Vertical Gaussian Doping Profile," in the proceedings of 2016 IEEE International Conference On Recent Trends In Electronics Information Communication Technology (RTEICT), 2016, pp. 675–679. DOI: 10.1109/RTEICT.2016.7807930

9. Shashi Kala Nagarkoti, **Balraj Singh**, and Manoj Kumar, "An algorithm for fetal heart rate detection using wavelet transform," in the proceedings of 2012 IEEE 1st International Conference on Recent Advances in Information Technology (RAIT), 2012, pp. 838–840. **DOI:** 10.1109/RAIT.2012.6194533

10. **Balraj Singh**, Shashi Kala Nagarkoti, and Brajesh Kumar Kaushik, "A modified algorithm for maternal heart rate detection using RR interval," in Proceedings of 2011 IEEE International Conference on Emerging Trends in Networks and Computer Communications, ETNCC2011, 2011, no. 1, pp. 39–42. **DOI:** 10.1109/ETNCC.2011.5958482

<table>
<tr><td>Books Authored/Book Volume Chapters</td><td colspan="3"></td></tr>
<tr><td rowspan="3">No. of Conferences</td><td rowspan="2">National</td><td>Attended</td><td>Organized</td></tr>
<tr><td>-</td><td>-</td></tr>
<tr><td>International</td><td>7</td><td></td></tr>
<tr><td rowspan="3">Research Guidance</td><td rowspan="2">Awarded</td><td>PG</td><td>Doctorate</td></tr>
<tr><td>4</td><td>1</td></tr>
<tr><td>Undergoing</td><td>-</td><td>2</td></tr>
<tr><td rowspan="2">Research Projects</td><td>Completed</td><td colspan="2">0</td></tr>
<tr><td>Undergoing (March,2023 to March 2026)</td><td colspan="2">Core Research Grant of 30 Lac received from Science and Engineering Research Board (SERB) for Project titled "Exploration and Design Optimization of Negative Capacitance Nanosheet Field Effect Transistor for Memory and Analog Applications.</td></tr>
<tr><td>Awards & Distinctions</td><td colspan="3"></td></tr>
<tr><td>Administrative Assignments Handled</td><td colspan="3">Coordinator, Incubation Cell, Start-up and Entrepreneurship Cell, G. B. Pant Institute of Engineering and Technology, Pauri Garhwal, from13/02/ 2023 to till date.
Controller Examination, G. B. Pant Institute of Engineering and Technology, Pauri Garhwal, from 5/03/ 2018 to till date.
Warden, Badri Hostel (120 Seated Hostel) from 01/02/2017 to 27/06/2020
Officer in Charge, Communication, G. B. Pant Engineering College, Pauri Garhwal, from 27 /07 2011 to 19/07/2013.
Team Manager, ECE Team, G. B. Pant Engineering College, Pauri Garhwal, from Oct 2010 to 2013 date.
Warden, krdar (C+D), G. B. Pant Engineering College, Pauri Garhwal, from 21/11/2011 to 19/07/ 2013
Asst. Warden, krdar (C+D), G. B. Pant Engineering College, Pauri Garhwal, from 13/07/2011 to 21/11/ 2011.
8. Asst. Warden, Raman Hostel G. B. Pant Engineering College, Pauri Garhwal, from 06/05 2010 to 13/07/2011.
9. Member Campus wide networking, G. B. Pant Engineering College,</td></tr>
</table>

	Pauri Garhwal, 2012.
Association with Professional Bodies	Senior Member IEEE
Any other Achievements	

Dr. Balraj Singh